HB56A1636B/SB-6B/7B/8B

16,777,216-word × 36-bit High-Density Dynamic RAM Module

HITACHI

ADE-203-591A(Z)
Rev. 1.0
05/10/96

Description

The HB56A1636 is a 16-Mbit × 36 dynamic RAM module, consisting of 36 16-Mbit DRAMs (HM5116100BS) sealed in an SOJ package.

The HB56A1636 enclosed in a 72-pin single in-line package. Therefore, the HB56A1636 makes high-density mounting possible without surface mount technology. The HB56A1636 provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ on the module board.

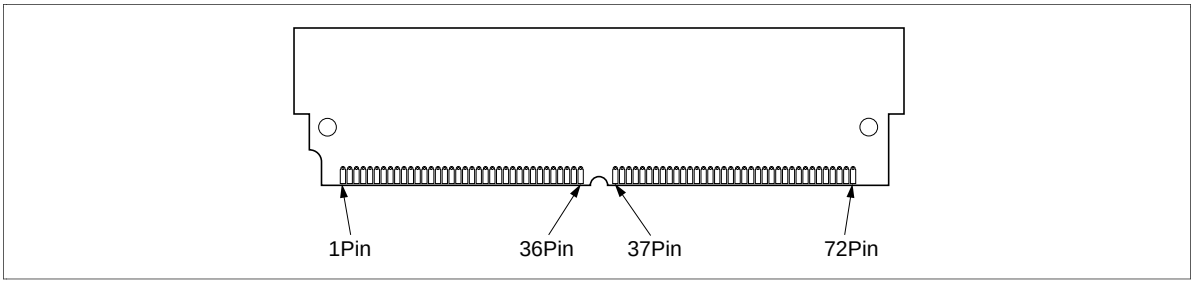
Features

- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - Access time: t_{RAC} = 60/70/80 ns (max)
  - Access time: t_{CAC} = 15/18/20 ns (max)
- Low power dissipation
  - Active mode: 15.2/13.3/12.3 W (max)
  - Standby mode (TTL): 378 mW (max)
  - Standby mode (CMOS): 189 mW (max)
- Fast page mode capability
- 4,096 refresh cycles: 64 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56A1636B-6B	60 ns	72-pin SIP socket type	Gold
HB56A1636B-7B	70 ns	72-pin SIP socket type	Gold
HB56A1636B-8B	80 ns	72-pin SIP socket type	Gold
HB56A1636SB-6B	60 ns	72-pin SIP socket type	Solder
HB56A1636SB-7B	70 ns	72-pin SIP socket type	Solder
HB56A1636SB-8B	80 ns	72-pin SIP socket type	Solder

Pin Arrangement



Pin Arrangement

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	A10	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	A11	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

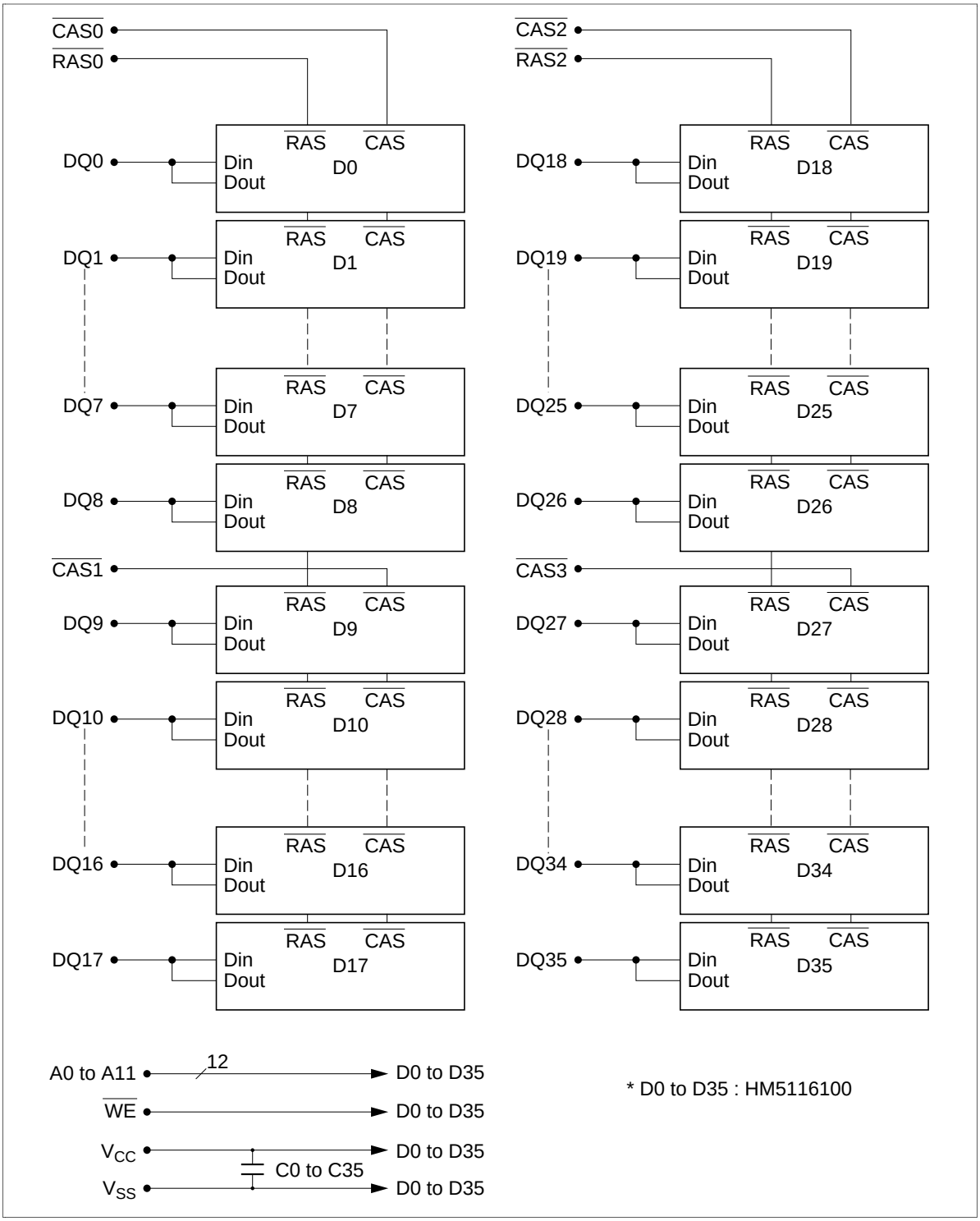
Pin Description

Pin Name	Function
A0 to A11	Address input: A0 to A11 Row address: A0 to A11 Column address: A0 to A11 Refresh address: A0 to A11
DQ0 to DQ35	Data-in/data-out
$\overline{RAS0}$, $\overline{RAS2}$	Row address strobe
$\overline{CAS0}$ to $\overline{CAS3}$	Column address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 to PD4	Presence detect pin
NC	Non-connection

Presence Detect Pin Arrangement

Pin No.	Pin Name	60 ns	70 ns	80 ns
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	V_{SS}	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	36	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
Supply voltage	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		60 ns		70 ns		80 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test condition**	**Note**
Operating current	I_{CC1}	—	2880	—	2520	—	2340	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	72	—	72	—	72	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
Standby current	I_{CC2}	—	36	—	36	—	36	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	2880	—	2520	—	2340	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	180	—	180	—	180	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	2880	—	2520	—	2340	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	2520	—	2160	—	1800	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7.0 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7.0 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected; I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	195	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	267	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	146	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	83	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	25	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or other effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)[*1, *2]

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write and Refresh Cycles (Common parameters)

		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	18	10000	20	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	52	20	60	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	5
Refresh period (4,096 cycles)	t_{REF}	—	64	—	64	—	64	ms	

Read Cycle

		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	18	—	20	ns	7, 8, 15
Access time from address	t_{AA}	—	30	—	35	—	40	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	30	—	35	—	40	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	—	15	ns	11
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	

Write Cycle

		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	12
Write command hold time	t_{WCH}	10	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	13
Data-in hold time	t_{DH}	10	—	15	—	15	—	ns	13

Refresh Cycle

		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	

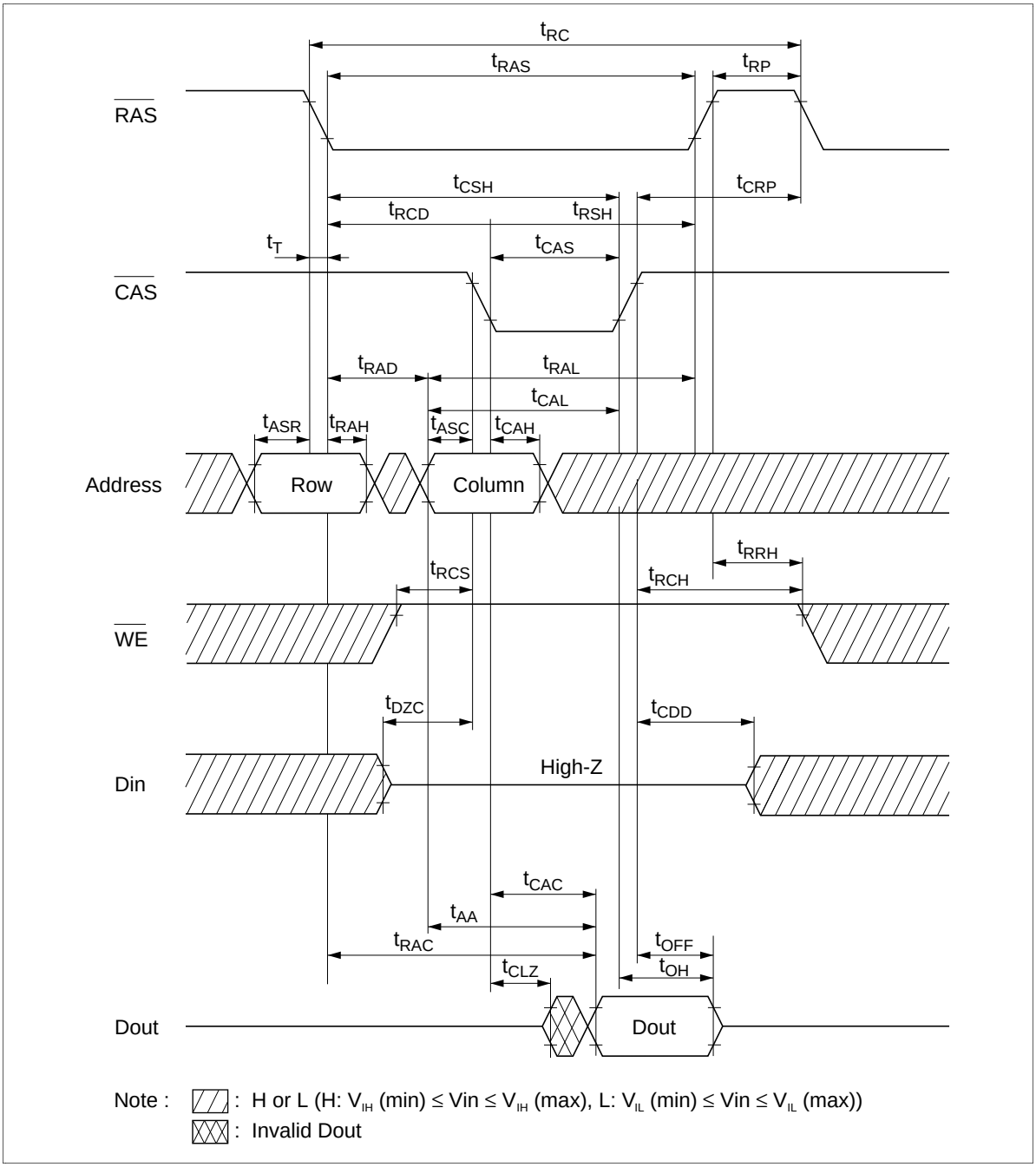
Fast Page Mode Cycle

		60 ns		70 ns		80 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	—	45	ns	7, 15
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	45	—	ns	

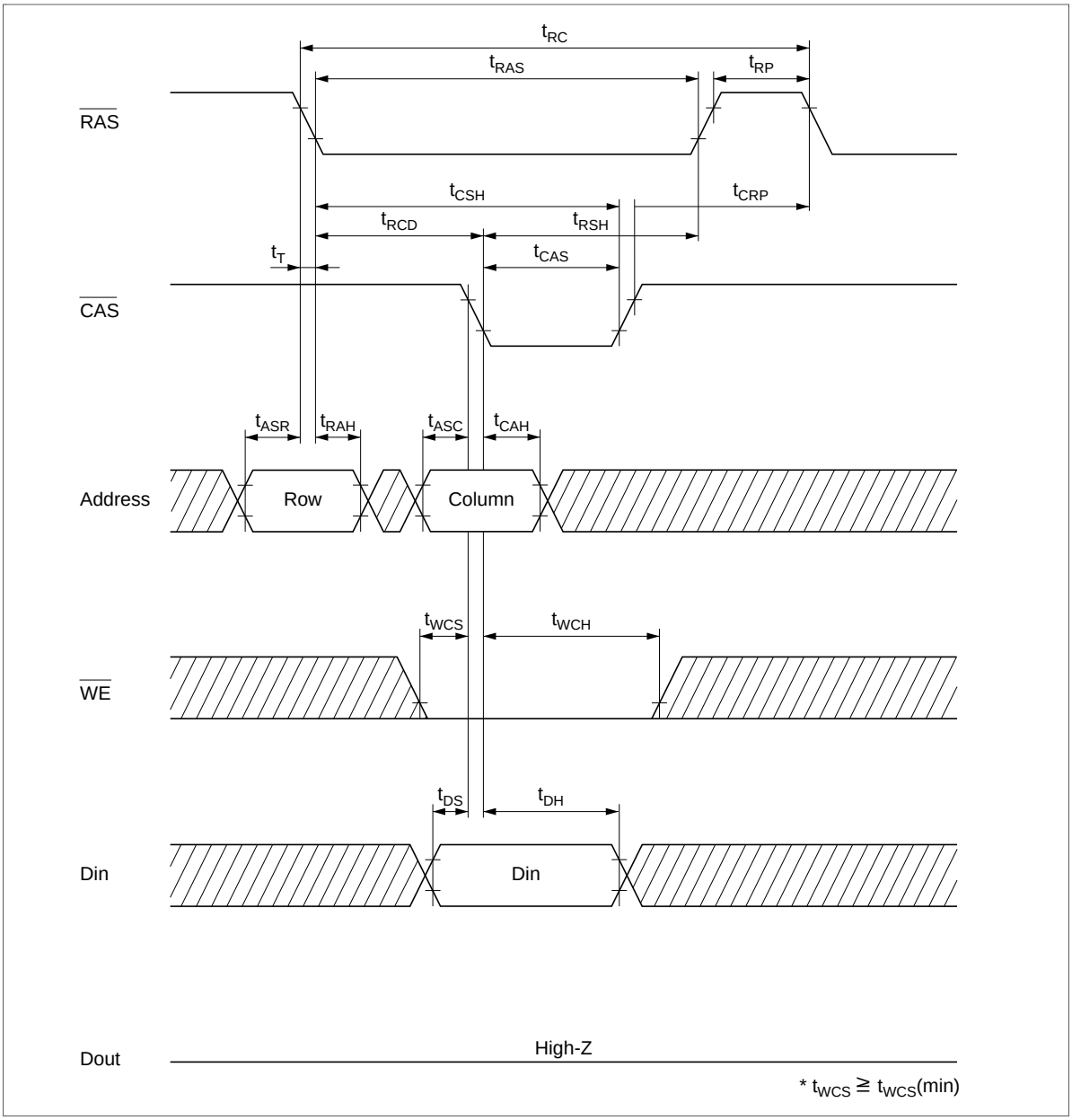
Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
12. t_{WCS} is not restrictive operating parameters. It is included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
15. Access time is determined by the longest among t_{AA} or t_{CAC} and t_{CPA}.

Timing Waveforms

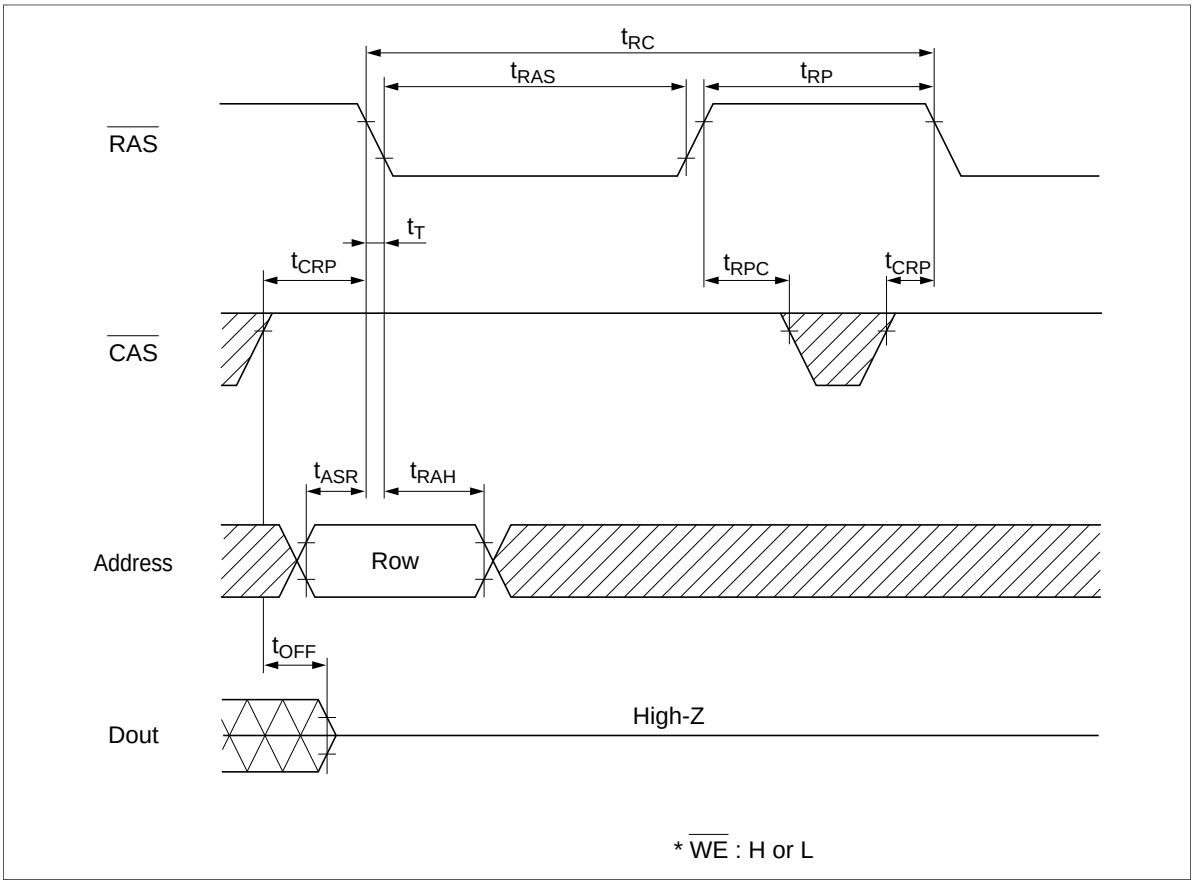
Read Cycle



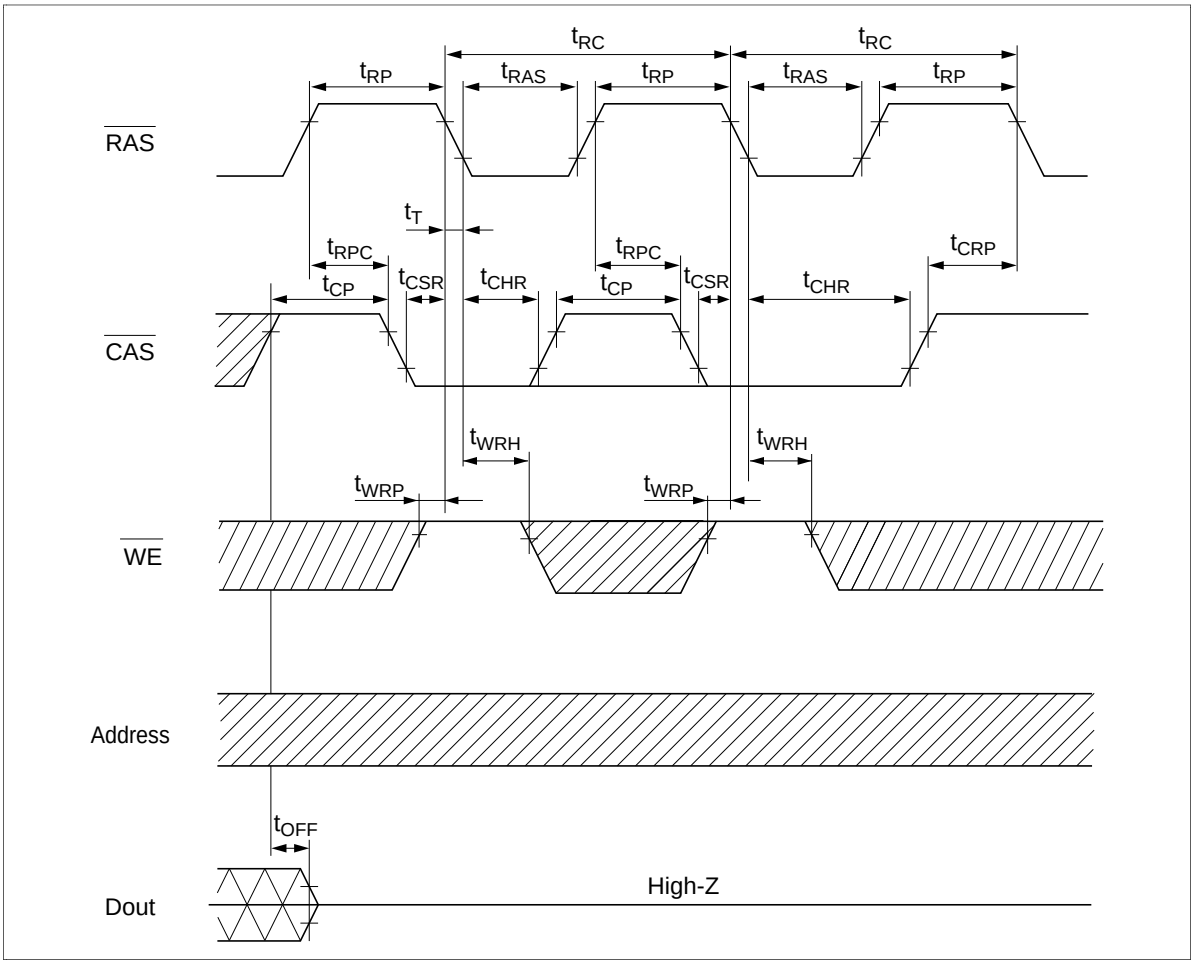
Early Write Cycle



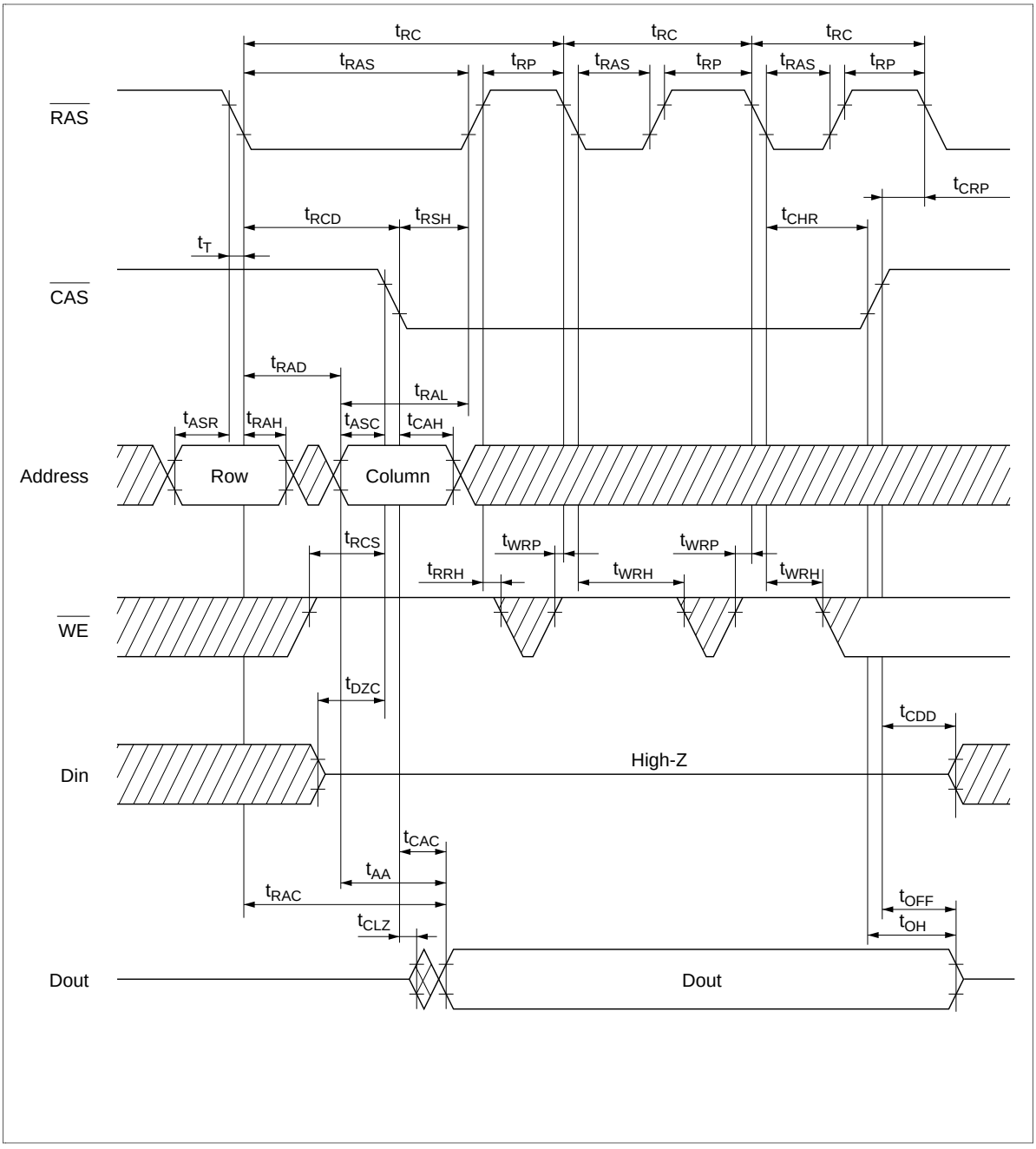
$\overline{\text{RAS}}$-Only Refresh Cycle



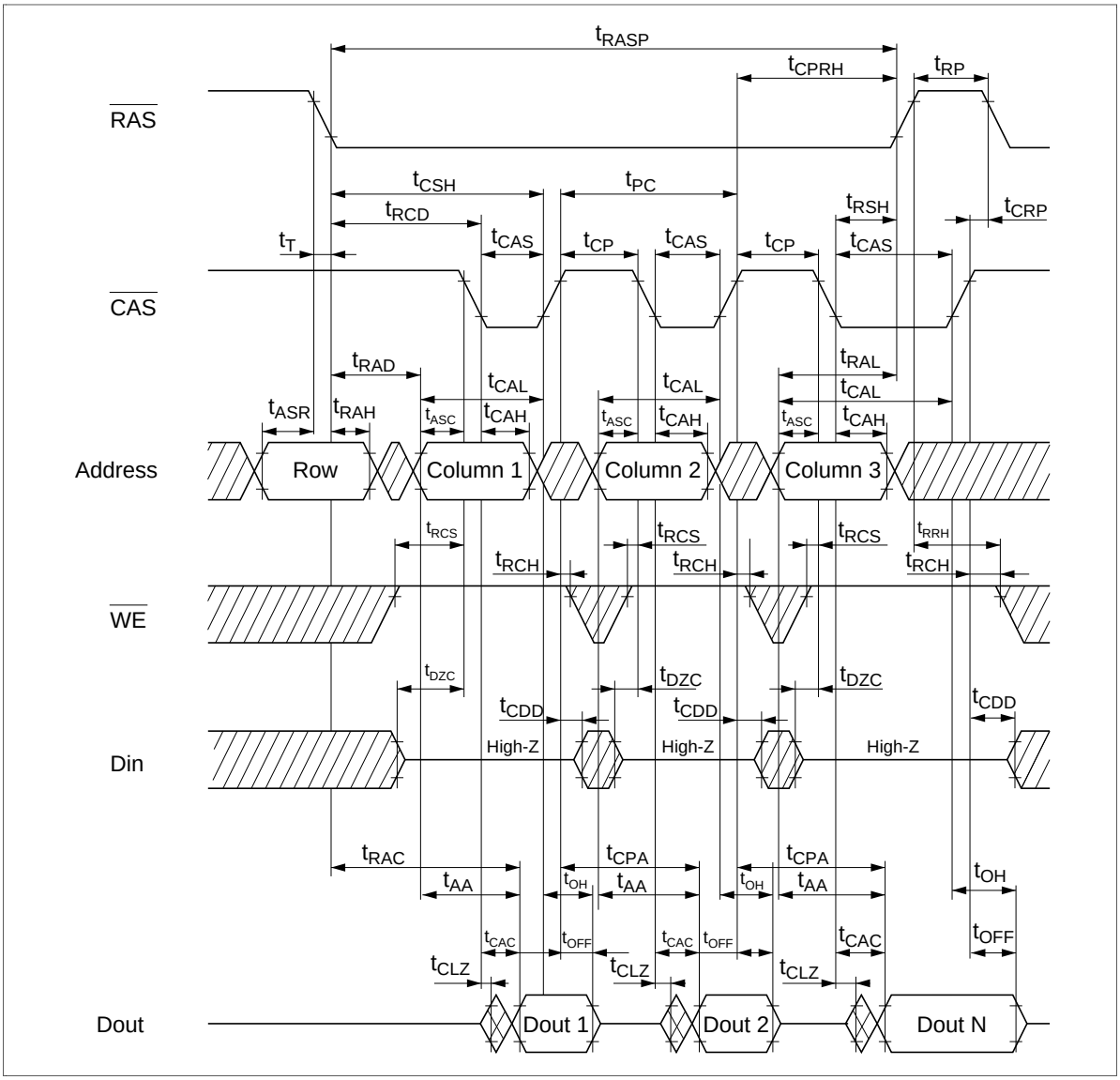
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



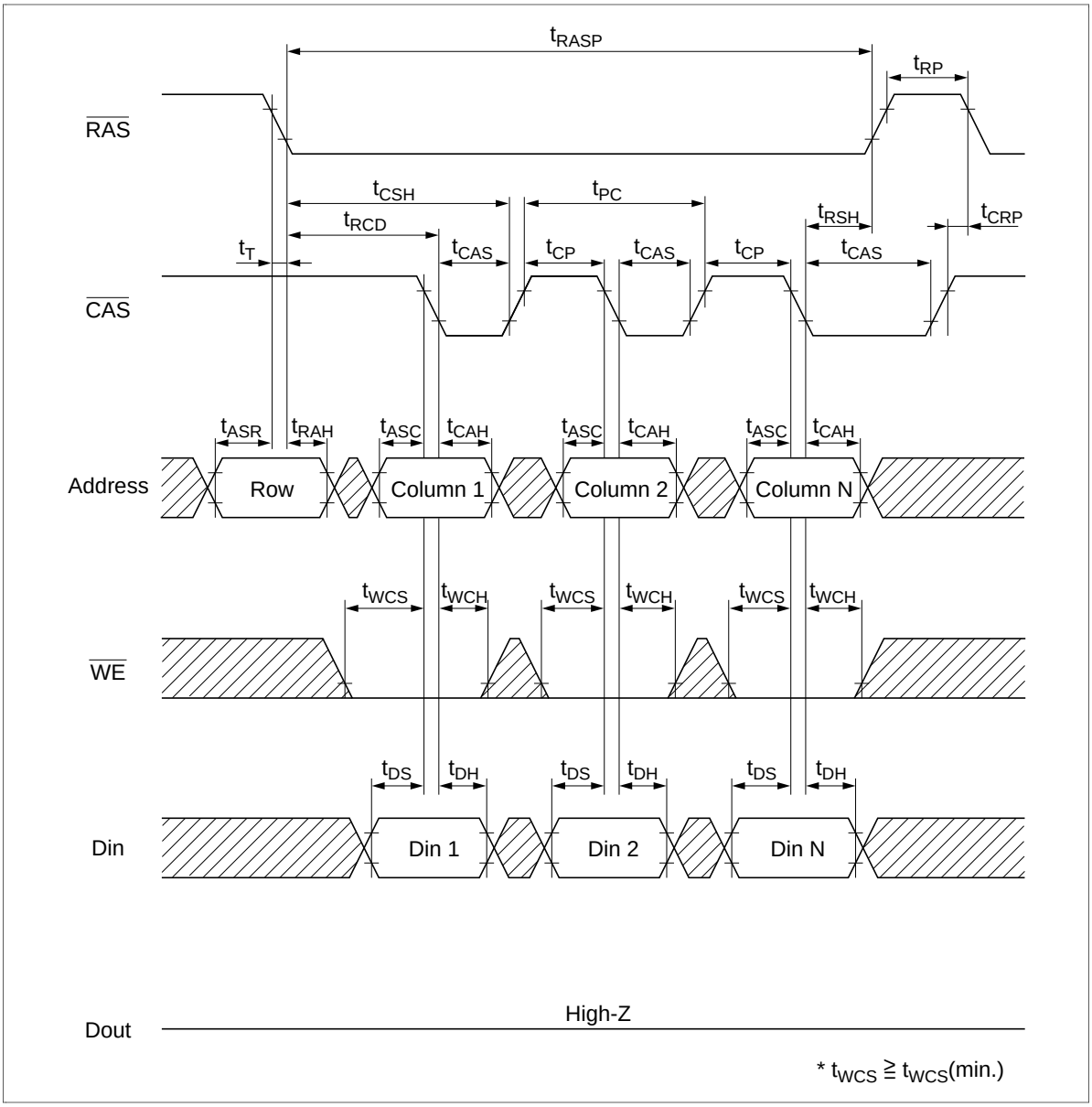
Hidden Refresh Cycle



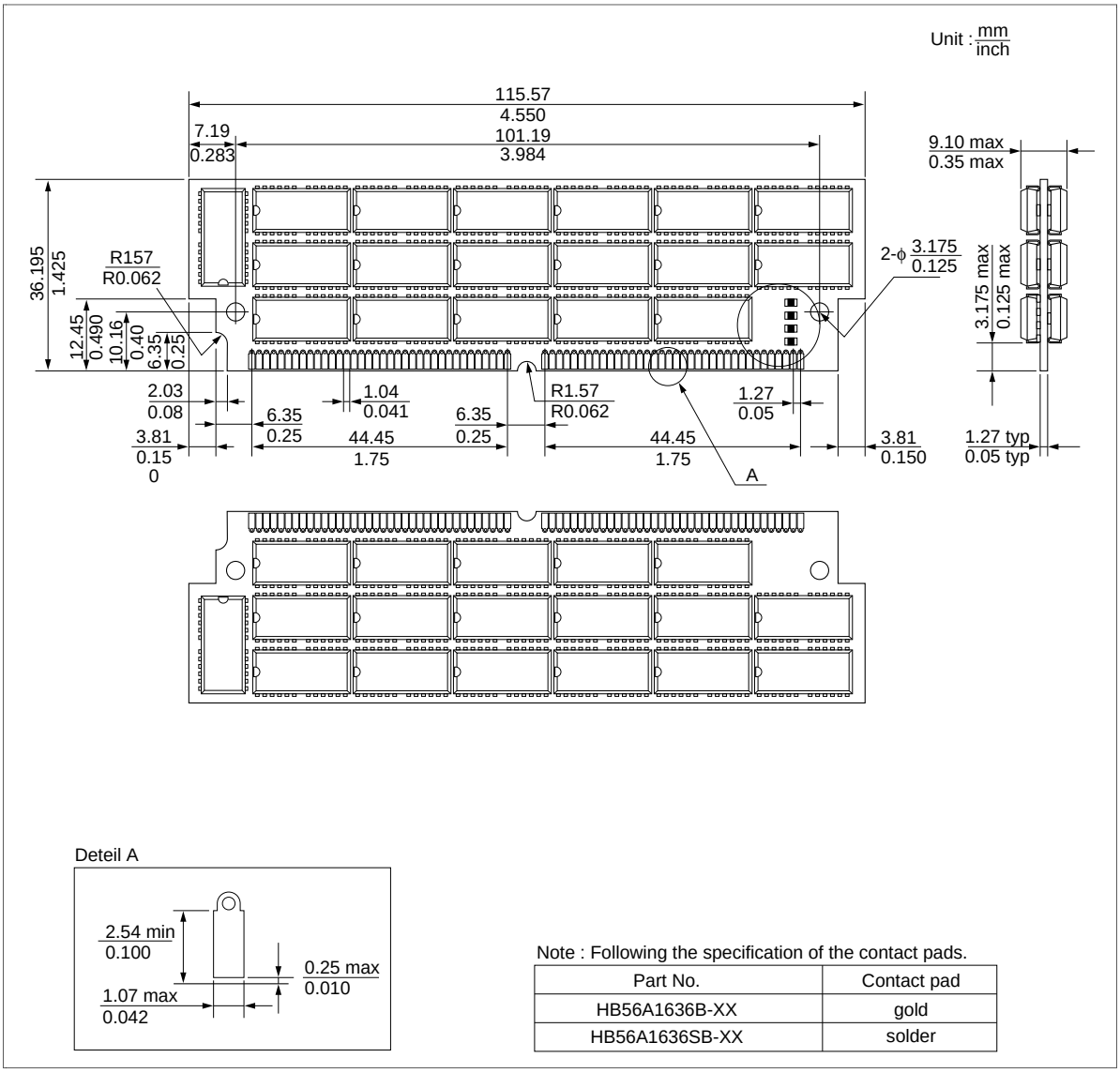
Fast Page Mode Read Cycle



Fast Page Mode Eary Write Cycle



Physical Outline



Note : Following the specification of the contact pads.

Part No.	Contact pad
HB56A1636B-XX	gold
HB56A1636SB-XX	solder